While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations which fall within the spirit and scope of the included claims. All matters set forth herein or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

THE INVENTION CLAIMED IS:

1. A processing mechanism for processing unprocessed micro devices into processed micro devices, comprising:

a processor for generating address signals, data signals and control signals;

a pin driver module coupled to the processor;

a backplane module coupled to the pin driver module; and

at least one socket coupled to the backplane module, the at least one socket for placement of the unprocessed micro devices; wherein:

the pin driver module routes the address signals, data signals and control signals to the backplane module, and provides a first plurality of voltages to the backplane module;

the backplane module routes the address signals, data signals and control signals to the at least one socket, and provides a second plurality of voltages to the at least one socket.

2. The processing mechanism as claimed in claim 1 wherein:

the pin driver module includes:

a logic circuit for routing the address signals, data signals and control signals to the backplane module, and

a voltage source circuit for providing the first plurality of voltages to the buffer circuit.

3. The processing mechanism as claimed in claim 1 wherein:

the backplane module includes:

a relay switch circuit for routing the address signals, data signals and control signals to the at least one socket, and

a buffer circuit for providing the second plurality of voltages to the at least one socket.

4. The processing mechanism as claimed in claim 2 wherein the logic circuit includes a field programmable gate array.

5. The processing mechanism as claimed in claim 2 wherein the voltage source circuit includes a digital to analog converter.

6. The processing mechanism as claimed in claim 2 wherein the first plurality of voltages includes a $V_{CC}$ voltage and a processing voltage for processing the unprocessed micro devices.

7. The processing mechanism as claimed in claim 2 wherein the first plurality of voltages includes a $V_{pp}$ voltage and a processing voltage for processing the unprocessed micro devices.

8. A processing mechanism for processing unprocessed micro devices into processed micro devices, comprising:

a processor for generating address signals, data signals and control signals;

a pin driver module coupled to the processor, the pin driver module including a logic circuit and a voltage sources circuit;

a backplane module coupled to the pin driver module, the backplane module including a relay switch circuit and a buffer circuit; and

at least one socket coupled to the backplane module, the at least one socket for placement of the unprocessed micro devices; wherein:

the logic circuit routes the address signals, data signals and control signals to the backplane module, and the voltage source circuit provides a first plurality of voltages to the buffer circuit;

the relay switch circuit routes the address signals, data signals and control signals to the at least one socket, and the buffer circuit provides a second plurality of voltages to the at least one socket.

9. The processing mechanism as claimed in claim 8 wherein the logic circuit includes a field programmable gate array.

10. The processing mechanism as claimed in claim 8 wherein the voltage source circuit includes a digital-to analog converter.

11. The processing mechanism as claimed in claim 8 wherein the first plurality of voltages includes a $V_{CC}$ voltage and a processing voltage for processing the unprocessed micro devices.

12. The processing mechanism as claimed in claim 8 wherein the first plurality of voltages includes a $V_{pp}$ voltage and a processing voltage for processing the unprocessed micro devices.

13. A buffer circuit for a processing mechanism capable of processing unprocessed micro devices into processed micro devices, the processing mechanism having a processor for generating control data signals and processing data signals and for receiving device data signals, a voltage reference source for providing a voltage reference, and a $V_{CC1}$ voltage supply for providing a $V_{CC1}$ voltage, and at least one socket for placement of the

unprocessed micro devices, the programming data signals are of $V_{CC1}$ volt logic levels, comprising:

a digital-to-analog converter (DAC) coupled to the processor and the voltage reference source, the DAC responsive to the control data signals and the voltage reference to generate a first variable DC voltage;

an amplifier coupled to the DAC, the amplifier responsive to the first variable DC voltage to generate a second variable DC voltage; and

a level-shifting translating buffer coupled to the amplifer, the processor, the $V_{CC1}$ voltage supply, and the socket for transferring processing data signals from the processor to the unprocessed micro devices and for transferring the device data signals from the processed micro devices to the processor, the level-shifting translating buffer responsive to the $V_{CC1}$ voltage and the second variable DC voltage to provide a plurality of logic levels for the device data signals.

14. The buffer circuit as claimed in claim 13 wherein the first variable voltage has a value between 0 volt and the voltage reference.

15. The buffer circuit as claimed in claim 13 wherein the amplifier is an operational amplifier.

16. The buffer circuit as claimed in claim 13 wherein the plurality of logic levels is between 0 volts and $V_{CC1}$ volts.

17. A method for programming a programmable micro device using a processor, the programmable micro device having a plurality of memory locations for storing data, the memory locations being identified by a respective plurality of addresses, the programmable micro device being coupled to the processor via an address bus, a data bus and a control bus, comprising the steps of:

(a) providing a first address from the processor to the programmable micro device over the address bus;

(b) providing a first data corresponding to the first address from the processor to the programmable micro device over the data bus; and

(c) providing a first control signal from the processor to the programmable micro device over the control bus to enable the programmable micro device to accept the first data from the processor at a memory location identified by the first address in the programmable micro device.

18. The method as claimed in claim 17 including the steps of:

(d) providing a second control signal from the processor to the programmable micro device over the control bus to enable the programmable micro device to provide to the processor data stored in the memory location identified by the first address over the data bus; and

(e) comparing the data stored in the memory location identified by the first address in the programmable micro device with the first data.

19. The method as claimed in claim 18 including the steps of:

(f) repeating steps (a) through (e) when the data stored in the memory location identified by the first address in the programmable micro device is not identical to the first data.

20. The method as claimed in claim 19 including the steps of:

(g) providing a signal by the processor to indicate a programming failure when, after repeating steps (a) through (e) for a predetermined number (N) of times, the data stored in the memory location identified by the first address in the programmable micro device is still not identical to the first data, wherein N is an integer.

21. A method for reading a programmable micro device using a processor, the programmable micro device having a plurality of memory locations for storing data, the memory locations being identified by a respective plurality of addresses, the programmable micro device being coupled to the processor via an address bus, a data bus and a control bus, comprising the steps of:

(a) providing a first address from the processor to the programmable micro device over the address bus; and

(b) providing a first control signal from the processor to the programmable micro device over the control bus to enable the programmable micro device to provide a first data from a memory location identified by the first address in the programmable micro device over the data bus.

22. A programming mechanism capable of programming unprogrammed micro devices into programmed micro devices, the programmed micro devices having a plurality of memory locations for storing data, the plurality of memory locations being identified by a respective plurality of addresses, comprising:

a plurality of sockets for placement of processed micro devices;

a plurality of data buffer/registers, each of the plurality of data buffer/registers coupled to a respective one of the plurality of sockets for receiving a first data stored in a first address in each of the programmed micro devices;

a plurality of compare circuits, each of the plurality of compare circuits having a first input and a second input and one output, the first input of each of the plurality of compare circuits being coupled to a respective one of the data buffer/registers for receiving the first data;

an expected data register coupled to the second input of each of the respective plurality of compare circuits for providing a first expected data;

a processor bus; and

a processor coupled to output of each of the plurality of compare circuits over the processor bus, wherein each of the compare circuits provides a first logic level at the output when the first data matches with the first expected data, and provides a second logic level at the output when the first data does not match with the first expected data.

23. The programming mechanism as claimed in claim 22 wherein the compare circuits are exclusive OR gates.

24. A method for verifying data programmed in a plurality of programmed micro devices using a programming mechanism capable of programming unprogrammed micro devices into programmed micro devices, the programmed micro devices having a plurality of memory locations for storing data, the plurality of memory locations being identified by a respective plurality of addresses, comprising steps of:

(a) providing to each of a plurality of data buffer/registers a first data stored in a first address in each of the plurality of programmed micro devices;

(b) providing the first data to a first input of each of a plurality of compare circuits;

(c) providing a first expected data from an expected data register to a second input of each of the plurality of compare circuits;

(d) comparing the first data with the first expected data using the plurality of compare circuits;

(e) outputting a first logic level at an output of a respective one of the plurality of compare circuits when the first data matches with the first expected data, and

(f) outputting a second logic level at the output of a respective one of the plurality of compare circuits when the first data does not match with the first expected data.

25. The method as claimed in claim 24 including the steps of:

(g) identifying, after step (f), the programmed micro devices that include the first data which does not match with the first expected data by detecting a logic level at the output of the plurality of compare circuits.

26. The method as claimed in claim 25 including the steps of:

(h) programming, after step (g), the programmed micro devices when the programmed micro devices include the first data which does not match with the first expected data.

27. The method as claimed in claim 25 including the steps of:

(i) rejecting, after step (g), the programmed micro devices when the programmed micro devices include the first data which does not match with the first expected data.

28. The method as claimed in claim 25 including the steps of:

(j) repeating steps (a) to (f) for a second data stored in a second address in each of the plurality of programmed micro devices.